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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,867	03/17/2004	Jun Otsuka	Q79598	1991

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
HA, NGUYEN T	
ART UNIT	**PAPER NUMBER**
2831	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,867	OTSUKA ET AL.	
	Examiner	Art Unit	
	Nguyen T. Ha	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *11-22* is/are withdrawn from consideration.

5)☒ Claim(s) *3-10* is/are allowed.

6)☒ Claim(s) *1,2 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The examiner acknowledges the applicant's submission of the amendment dated 11/29/2006. At this point, claims 1-4 have been amended, claims 11-22 have been canceled, and claims 23-26 have been added. Thus, claims 1-10, and 23-26 are pending in the instant application.

Election/Restrictions

2. Claims 6-7 are directed to an allowable product. Pursuant to the procedures set forth in MPEP § 821.04(B), previously withdrawn from consideration as a result of a restriction requirement, claims 6-7 hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Response to Arguments

3. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 23-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakravorty et al. (US 6,775,150).

Regarding claim 23, Chakravorty et al. disclose a capacitor (figure 3) comprising:

- an approximately plate-shaped capacitor (141 &151) main body having a first ceramic surface on which semiconductor device (60) having surface-connecting terminals is to be mounted and a second surface, and
- a plurality of electrically conductive vias (107 & 143 & 153) penetrating the capacitor main body between the first and second surfaces for connection with the surface-connecting terminals.

Regarding claim 24, Chakravorty et al. disclose a semiconductor device equipped capacitor assembly (figure 3) comprising:

- a semiconductor device (60) having surface-connecting terminals, and
- a capacitor (90) having an approximately plate-shaped capacitor main body having a first ceramic surface on which the semiconductor device is mounted and a second surface and a plurality of electrically conductive vias (107 &143 & 153) penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting terminals.

Regarding claim 25, Chakravorty et al. a capacitor equipped substrate assembly comprising:

- a substrate (200) having surface-connecting pads;
- a capacitor (90) having an approximately plate-shaped capacitor main body having a first ceramic surface and a second surface at which the

capacitor is mounted on the substrate and a plurality of electrically conductive vias (107 &143 & 153) penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting pads.

Regarding claim 26, Chakravorty et al. disclose an assembly (figure 3) comprising:

- a semiconductor device (60) having surface-connecting terminals;
- a substrate (200) having surface-connecting pads; and

a capacitor (90) having an approximately plate-shaped capacitor main body having a first ceramic surface on which the semiconductor device is mounted and a second surface at which the capacitor main body is mounted on the substrate and a plurality of electrically conductive vias (107 &143 & 153) penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting terminals and the surfaces-connecting terminals and the surface-connecting pads.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty et al. (US 6,775,150) in view of Farooq et al. (US 6,072,690).

Regarding claim 1, Chakravorty et al. disclose a capacitor (figures 1-3) comprising:

- an approximately plate-shaped capacitor main body (90) having a first surface on which a semiconductor device (60) having surface-connecting terminals (121 & 125) is to be mounted and a second surface; and
- a plurality of electrically conductive vias (143 & 153) penetrating the capacitor main body (90) between the first and second surfaces for connection with the surface connecting terminals.

Chakravorty et al. fail to teach the plurality of electrically vias all have a straight shape.

Farooq et al. teach a plurality of electrically vias (64-66) having a straight shape (figure 3A).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the assembly as taught by Farooq et al. in to Chakravorty et al., to do so, it would add significant capacitance and coupling parasitic to the device.

Regarding claim 2, Chakravorty et al. disclose a semiconductor device equipped capacitor assembly (figures 1-3) comprising:

- a semiconductor device (60) having surface-connecting terminals (121 & 125); and
- a capacitor (90) having an approximately plate-shaped capacitor main body having a first surface on which the semiconductor device is mounted and a second surface and a plurality of electrically conductive vias (143 & 153) penetrating the capacitor main body between the first and second surfaces and connected to the surface-connecting terminals.

Chakravorty et al. fail to teach the plurality of electrically vias all have a straight shape.

Farooq et al. teach a plurality of electrically vias (64-66) having a straight shape (figure 3A).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the assembly as taught by Farooq et al. in to Chakravorty et al., to do so, it would add significant capacitance and coupling parasitic to the device.

Allowable Subject Matter

8. Claims 3-10 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claims 3-4, the prior art alone or in combination does not teach the limitation of a capacitor equipped substrate assembly comprising a substrate and a capacitor, wherein the thermal expansion coefficient of the capacitor main body is

smaller than that of the substrate. With respect to claims 5-7, the prior art alone or in combination does not teach the limitation of an interposer comprising an interposer main body having a first surface on which a semiconductor device having surface-connecting terminals is mounted and a second surface formed with a recess, and a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between the first surface and a bottom surface of the recess and connected to the surface-connecting terminals. With respect to claim 8, the prior art alone or in combination does not teach the limitation of a semiconductor device equipped interposer assembly comprising: an interposer main body having a first surface on which the semiconductor device having surface-connecting terminals is mounted and a second surface formed with a recess, and capacitor disposed in the recess and having front and rear surfaces and a plurality of capacitor side electrically conductive vias extending through the front and rear surfaces. With respect to claim 9, the prior art alone or in combination does not teach the limitation of an interposer equipped substrate assembly comprising an interposer having a plurality of interposer main body side electrically conductive vias penetrating the interposer main body between first and second surfaces and connected to the surface-connecting terminal and a capacitor disposed in the recess. With respect to claim 10, the prior art alone or in combination does not teach the limitation of an assembly comprising an interposer having an approximately plate shaped interposer main body having a first surface on which the semiconductor device is mounted and a second surface formed with a recess, and the interposer further having a plurality of interposer main body side electrically

conductive vias penetrating the interposer main body between the first surface and a bottom surface of the recess and connected to the surface-connecting terminals and a capacitor disposed in the recess.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-

1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NGUYEN T. HA
PRIMARY EXAMINER

NH
February 20, 2007